UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,110	10/26/2001	Tod David Wolf	TI-33162	7695

7590 06/04/2004

Ronald O. Neerings
Texas Instruments Incorporated
M/S 3999
P.O. Box 655474
Dallas, TX 75265

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRL

Office Action Summary	Application No. 10/033,110	Applicant(s) WOLF ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 18-23* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/26/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

1. Claims **11-17** drawn to generating operands through logic gates and determining original operands classified in 708/550.
2. Claims **1-10 and 18-23,** drawn to decoding and producing extrinsic data in response to operands classified in 714/755.

The invention are distinct, each from the other because of the following reasons: Invention Group 1 and group 2 are unrelated. Inventions are unrelated if it can be shown that they are not disclosed at capable of use together and they are different modes of operation, different functions or different effects (MPEP 806.04, MPEP 808.01). In the instant case for the different inventions; the invention group 1 is generating operands using logic gates and determining original operands which has a completely different functions, a completely different effect and a completely different mode of operation from the invention of group 2, a MAP decoder comprising beta and alpha blocks for producing state metrics in two's complement and producing extrinsic data. Because these inventions are distinct for the reason given above and the search required for the group 1 is not required for group 2, restricting for examination purposes as indicated is proper. Because these inventions are distinct for the reason given above and the search required for group 2 is not required for group 1, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Neerinngs Ronald on May 21, 2004 a provisional election was made without traverse to prosecute the invention of group II claims 1-10 and 18-23. The applicant in replying to this office action must make affirmation of this election. Claims 11-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

DETAILED ACTION

1. Claims **1-10 and 18-23** are remains for the examination. Applicant is reminded that the non-elected claims **11-17** are to be cancelled from the file on or at allowance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1 the word "thereof" on page 17 lines 4 renders the claim indefinite because the word "thereof" makes the claim language unclear. The examiner would appreciate if the applicant would clarify this matter.

Claim Rejections - 35 USC § 101

3. Claims **1-10** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter because:

As per claim **1**, the language of the claim (the method of preparing operands that are represented in two's complement format for use in binary arithmetic comprising the steps of determining maximum or negative values boundary associated with the two's complement format and adjusting the values if the original operands are not with in predetermined proximity) raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C 101.

Claims **2-10** which are directly or indirectly dependents of claim 1 are also rejected under 35 U.S.C 101.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims **1-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maru (U.S. PN: 6,516,444).

As per claims **1 and 2,** Maru in figure 2A teach or disclose an output from sum from an adder and a parity sequence are input to two's complement circuits (203 and 204) with control terminals wherein each of the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64). Further, Maru teaches that with this function, outputs from the complement circuits output negative values while holding their absolute values (see col. 4, lines 40-64). Maru **does not explicitly teach** a method of adjusting values when the values are within predetermined proximity. **However,** Maru teaches a method of combining output values from complement circuits (203 and 204) coupled by an adder (205) and further selected by four selectors (206-209) to enable selection and combinations are selected by a most significant bit (202) representing the polarity of input data (see col. 5, lines 32-45). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made

to adjust the output values of the two's complement by using an adder and selectors. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because adjusting values, which are within proximity, would guarantee accurate operations.

As per claims **3 and 4,** Maru teach all the subject matter claimed in claim 1 including the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64).

As per claims **5 and 6,** Maru teach all the subject matter claimed in claim 1 including in figure 2A teach an adder (205) for adding values.

As per claims 7 **and 8,** Maru teach all the subject matter claimed in claim 1 including in figure 8 teach a subtraction circuit for subtracting values (803).

As per claim **9,** Maru teach all the subject matter claimed in claim 1 including in figure 9 a turbo decoder

As per claim **10,** Maru teach all the subject matter claimed in claims 1 and 9 including in figure 9 a turbo decoder comprising an extrinsic information (see an output line from an element 907-1).

5. Claims **18-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art figure 4 in view of Maru (U.S. PN: 6,516,444).

As per claim 18, applicant's admitted prior art figure 4 teach a MAP decoder comprising an alpha block (see figure 4, alpha block) for producing alpha state metrics, a beta block (see figure 4, beta block), an extrinsic block (see figure 4, extrinsic block) coupled to alpha block and beta block for receiving metrics. Applicant's admitted prior art figure 4 **does not teach** an extrinsic block coupled to a logic gate (adder) to determine if an original value with in a predetermined value boundary or range associated with a 2's complement format. **However,** Maru in an analogous art teach a turbo decoder comprising a priori memory, an adder and selectors whereby the priori memory stores extrinsic/previous information in repetitive processing and the adder adds the information sequences, which the information will be selected by the selectors (see abstract and col. 1, lines 45-60). Further, Maru in figure 9 teaches that a result obtained by repeatedly using a soft decision output and a LOG likelihood from the SISO decoder (913) is finally subjected to hard decision by a decider (adjuster) (916) and returned to the original order by a de-interleaver (917), thereby obtaining decoded data (921) (see col. 3, lines 36-45). Furthermore, Maru in figure 2 teaches two 2's complement circuits (203, 204) coupled to the adder (205) and to the selectors (206-209) (see col. 5, lines 36-41). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of the applicant's admitted prior art to include logic gates coupled to the extrinsic block for adding, adjusting and producing an extrinsic data as taught by Maru. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to achieve a reduction in power consumption and an increase in speed of viterbi decoding operation (see col. 10, lines 33-44).

As per claims **19 and 20,** the applicant's admitted prior art in view of Maru teach all the subject matter claimed in claim 18 including Maru teaches that a hard decision by a decider (adjuster) (see figure 9, 916) obtaining decoded data (921) (see col. 3, lines 36-45). The applicant's admitted prior art in view of Maru **do not teach** none of the adjusting values are not with in the maximum positive and negative value boundary. **However**, setting or adjusting values "within" or "not within" the systems required range of values depends upon the designer's choice. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement or design any values within or not within the ranges. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so in order to permit flexibility in selection of the adjusted values.

As per claim **21,** the applicant's admitted prior art in view of Maru teach all the subject matter claimed in claim 18 including Maru in figure 9 teaches adders (904, 908 and 915) for adding values.

As per claim **22,** the applicant's admitted prior art in view of Maru teach all the subject matter claimed in claim 18 including Maru in figure 9 teaches previous information LOG likelihood and information sequence component, which are synchronized by delay units 912-1 and 912-2, are subtracted from the LOG likelihood by an adder 915, extrinsic information LOG likelihood 922 is generated.

As per claim **23,** the applicant's admitted prior art in view of Maru teach all the subject matter claimed in claim 18 and 22 including Maru in figure 9 teaches adders (904, 908 and 915) for adding values. Further, Maru teaches previous information LOG likelihood and information

sequence component, which are synchronized by delay units (912-1) and (912-2), are subtracted from the LOG likelihood by an adder 915, extrinsic information LOG likelihood (922) is generated.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,675,342 Yagyu

US PN: 6,715,120 Hladik et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

Guy J. Lamarre for

Albert DeCady
Primary Examiner